IN THE SPECIFICATION

Please amend the paragraph beginning on page 15, line 7 and extending to page 16, line 9 as suggested by the Examiner so the Specification conforms to amended FIG. 2 as follows:

FIG. 2 is a block diagram of power/performance controller 201. The description of power/performance controller 201 is found on page 15, line 7 through page 16, line 9. "FIG. 2 is a block diagram of a power/performance controller 201 according to embodiments of the present invention. Controller 201 may be either a state machine or a programmed controller executing a set of software instructions. Controller 201 receives physical parameters (outputs of various temperature sensors) 207 or other physical parameters 206 in first and second receiving circuits 210 and 211 respectively. Other physical parameters 206 may include, but are not limited to, acoustic noise levels, vibration levels, EMC noise levels, etc. Controller 201 also receives quality of service parameters 205. Quality of service parameters 205 may be parameters identifying guaranteed customer accessibility to processors, guaranteed bandwidth of processing, etc. Policy parameters 204 are values that define the cost of power, the availability of power, acceptable EMC levels, acoustic noise levels, etc. Logic or program instructions within controller 201 receive these parameters (204 through 207) and are configured to determine using third circuit 213 to sets of global and local controls 202 and 203, respectively. For example, all or a portion of parameter data 207 may include outputs 107 and 108 from multiprocessor VLSI chip 101. These controls are used to set using a fifth circuit 214 the various processors (e.g., 103, 104, 105, and 106) at power and performance levels by adjusting their supply voltages, clock frequencies, and cooling. The controls 202 and 203 may include signals that allow individual processors to be set to an operational or sleep mode. Embodiments of the present invention may implement controller 201 as with certain distributed functions. Controller 201 may issue some signals using a fourth circuit 212 to set an MP system to a certain global power level and additional control circuits in the MP system may determine how the power level is distributed between the individual processors in the MP system to achieve the global goal

and global MP system performance goals. For example, set points 109 and 110 may include one or more of controls 202 and 203.

Please amend the paragraph beginning on page 16, line 10 through page 17, line 6 as suggested by the Examiner so the Specification conforms to amended FIG. 3 as follows:

FIG. 3 is a block diagram illustrating the hierarchy and similarity of the various levels of multiprocessor systems. Multiprocessor VLSI chip 303 has inputs 308 and outputs 307 for controlling global and local chip parameters (e.g., temperatures, clock frequencies, and supply voltages). <u>A local cooling fan 322 and solid state cooling device 323 are shown on individual processor circuits on VLSI chip 303.</u> Several multiprocessor VLSI chips 303 are coupled on a printed circuit board (PCB) 302 and become part of a self-contained multiprocessor system (MS) 304 <u>with cooling fan 321</u> (e.g., a server). MS 304 also has global and local parameters and controls. MS 304 has a total (global) performance which is the summation of the performances of the individual processors on PCB 302. MS 304 also has a global temperature (e.g., air temperature inside the box). MS 304 also has local parameters associated with the individual performance of its various multiprocessor VLSI chips 303 and the individual processors on these chips. The temperatures of the individual VLSI chips 303 may be thought of as local to MS 304. Rack 301 <u>has cooling fans 320 and</u> may house many MS 304 units and likewise outputs local and global parameters (e.g., 206 and 207) which may be monitored by controller 201. Rack 301 may also receive local and global controls (e.g., 202 and 203) from controller 201. Cluster system 305 may house many racks 301 <u>and has a central cooling system 324</u>. Cluster system 305, similarly, receives local and global controls (e.g., 202 and 203) and outputs local and global parameters (e.g., 206 and 207).

Please amend paragraph beginning on page 13, line 3 and extending to page 14, line 3 as suggested by the Examiner as follows:

Embodiments of the present invention teach a common method of performance and power management which may be applied in different MP system environments. Various sensor data is used to measure physical parameters, and these physical

parameters are combined with policy and quality of service parameters to generate global and local actions for the various processor units in the multiprocessor environment. These actions include but are not limited to modifying the clock frequency and supply voltage of core logic in individual processor units on a multiprocessor VLSI chip, modifying the global frequency and supply voltage of I/O logic circuits, adjusting local cooling fan speed (e.g., added cooling fan 322) or active cooling devices (e.g., thermo-electric cooler 323) on individual VLSI chips, adjusting cooling fans on system level processing units (e.g., servers) with cooling fan 321), adjusting the cooling fans and air conditioning for multiple, stand-alone processing units (e.g., racks of servers with cooling system 324) and suspending operation (various modes of sleep ) of individual multiprocessor VLSI chips, stand-alone MP systems, or MP system clusters.